TLF4277-2

Low Drop Out Linear Voltage Regulator
Integrated Current Monitor

Data Sheet

Rev. 1.0, 2014-03-13

Automotive Power

Table of Contents

1 Overview . . . 3

2 Block Diagram . . . 4

3 Pin Configuration . . . 5
3.1 Pin Assignment . . . 5
3.2 Pin Definitions and Functions . . . 5

4 General Product Characteristics . . . 6
4.1 Absolute Maximum Ratings . . . 6
4.2 Functional Range . . . 7
4.3 Thermal Resistance . . . 7

5 Voltage Regulator . . . 8
5.1 Description Voltage Regulator . . . 8
5.2 Electrical Characteristics Voltage Regulator . . . 9
5.3 Application Information for setting the variable output voltage . . . 10
5.4 Typical Performance Characteristics Voltage Regulator . . . 11

6 Current Consumption . . . 12
6.1 Electrical Characteristics Current Consumption . . . 12
6.2 Typical Performance Graphs Current Consumption . . . 13

7 Current and Protection Monitor Functions . . . 14
7.1 Functional Description Current and Protection Monitors . . . 14
7.1.1 Linear Current Monitor . . . 15
7.1.2 Adjustable Output Current Limitation . . . 16
7.1.3 Overvoltage Detection . . . 16
7.1.4 Thermal Shutdown Detection . . . 16
7.1.5 Status Output Signal . . . 16
7.1.6 Typical Performance Graphs Current Monitor . . . 18

8 Enable Function . . . 19
8.1 Description Enable Function . . . 19
8.2 Electrical Characteristics Enable Function . . . 19

9 Application Information . . . 20
9.1 Application Diagram . . . 20
9.2 Selection of External Components . . . 20
9.2.1 Input Pin . . . 20
9.2.2 Output Pin . . . 20
9.3 Thermal Considerations . . . 21
9.4 Reverse Polarity Protection . . . 22
9.5 Further Application Information . . . 22

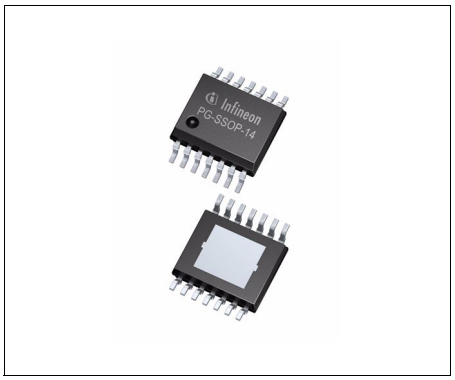
10 Package Outlines . . . 23

11 Revision History . . . 24

Low Drop Out Linear Voltage Regulator
Integrated Current Monitor

TLF4277-2EL

1 Overview



PG-SSOP14 EP

Features

- Integrated Current Monitor
- Overvoltage, Overtemperature and Overcurrent Detection
- Adjustable Output Voltage
- Output Current up to 300 mA
- Adjustable Output Current Limitation
- Very Low Current Consumption
- Very Low Dropout Voltage
- Stable with Ceramic Output Capacitor of 1 µF
- Wide Input Voltage Range up to 40 V
- Reverse Polarity Protection
- Short Circuit Protected
- Overtemperature Shutdown
- Automotive Temperature Range -40 °C ≤ T_j ≤ 150 °C
- Green Product (RoHS and WEEE compliant)
- AEC Qualified

Description

The TLF4277-2 is the ideal companion IC to supply active antennas for car infotainment applications. The adjustable output voltage makes the TLF4277-2 capable of supplying the majority of standard active antennas such as:

- FM/AM
- DAB
- XM
- SIRIUS

The TLF4277-2 is a monolithic integrated low drop out voltage regulator capable of supplying loads up to 300 mA. For an input voltage up to 40 V the TLF4277-2 provides an adjustable output voltage in a range from 5 V up to 12 V. The integrated current monitor function is a unique feature that provides diagnosis and system protection functionality. Fault conditions such as overtemperature and output overvoltage are monitored and indicated at the current sense output. The maximum output current limit of the device is adjustable to provide additional protection to the connected load.

Via the enable function the IC can be disabled to lower the power consumption. The PG-SSOP14 EP package provides an enhanced thermal performance within a SO8 body size.

Type	Package	Marking
TLF4277-2EL	PG-SSOP14 EP	4277-2

2 Block Diagram

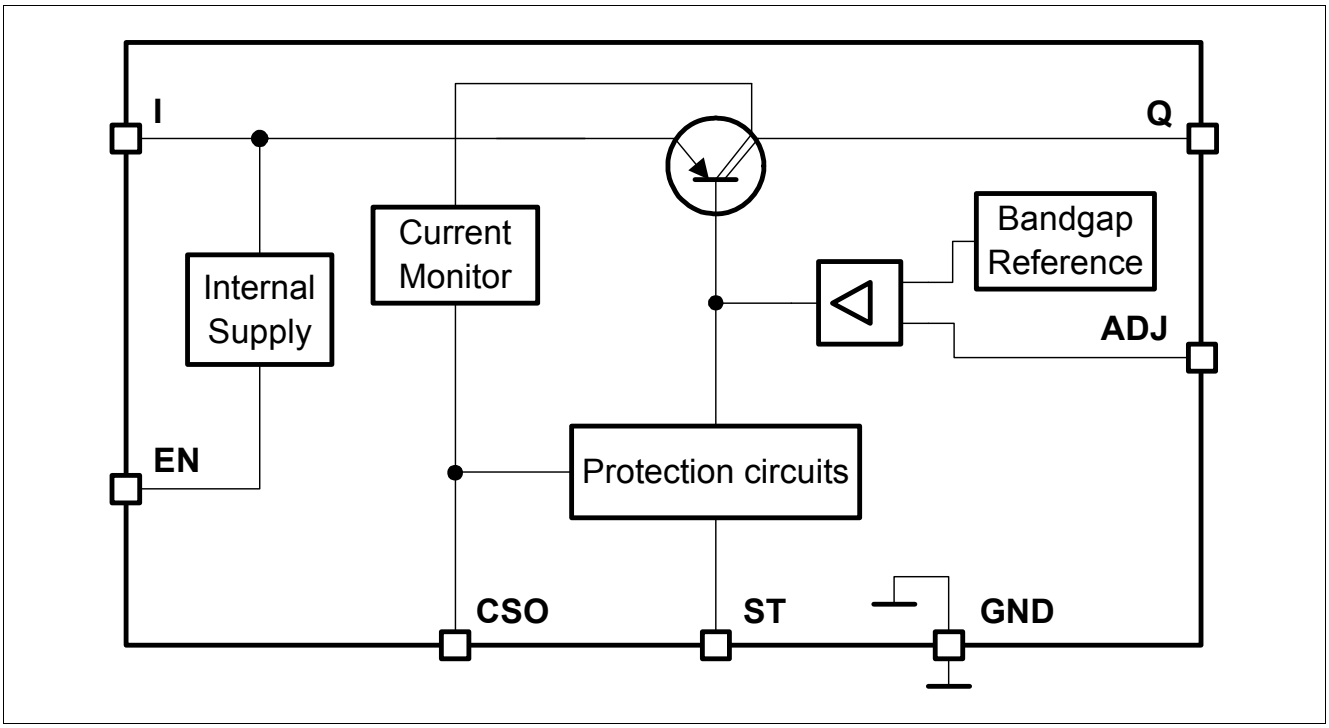


Figure 1 Block and simplified application diagram TLF4277-2 (Package PG-SSOP14 EP)

3 Pin Configuration

3.1 Pin Assignment

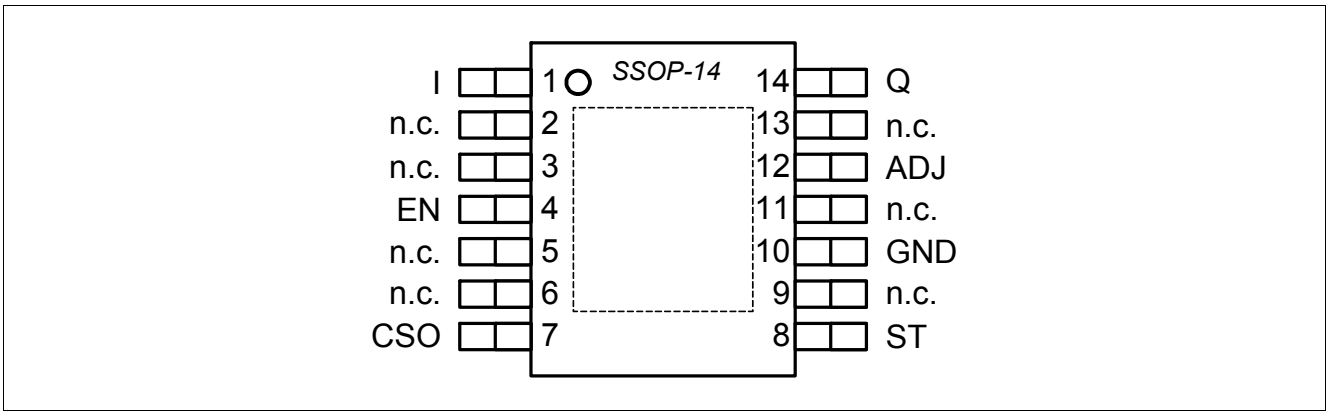


Figure 2 Pin Configuration (top view)

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	I	**IC Supply** Place a capacitor from I to GND close to the IC for compensating line influences.
4	EN	**Enable** High signal enables the regulator; Low signal disables the regulator; Connect to I, if the Enable function is not needed
7	CSO	**Current Sense Out** Current monitor and status output
8	ST	**Status Output** Digital output signal with open collector output. A low signal indicates fault conditions at the regulator‘s output.
10	GND	**Ground**
12	ADJ	**Voltage Adjust** Connect an external voltage divider to configure the output voltage
14	Q	**Regulator Output** Connect a capacitor between Q and GND close to the IC pins, respecting the values given for its capacitance C_Q and ESR in the table Chapter 4.2
	PAD	**Heat sink** Connect to PCB heat sink area and GND
2,3,5,6	n.c.	**Not Connected** Internally not connected; Connect to PCB GND
9,11,13	n.c.	**Not Connected** Internally not connected; Connect to PCB GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage Ratings							
IC Supply I	V_I	-16		45	V	–	P_4.1.1
Enable Input EN	V_{EN}	-16		45	V	–	P_4.1.2
Voltage Adjust Input ADJ	V_{ADJ}	-0.3		16	V	–	P_4.1.3
Regulator Output Q	V_Q	-0.3		45	V	$V_Q < V_I + 5$ V	P_4.1.4
Current Monitor Out CSO	V_{CSO}	-0.3		5	V	–	P_4.1.5
Status Output	V_{ST}	-0.3		45	V	2) see also **"Status Output Signal"**	P_4.1.6
Temperatures							
Junction Temperature	T_j	-40		150	°C	–	P_4.1.7
Storage Temperature	T_{stg}	-55		150	°C	–	P_4.1.8
ESD Susceptibility							
ESD Susceptibility to GND	V_{ESD}	-2		2	kV	HBM[3)]	P_4.1.9
ESD Susceptibility to GND	V_{ESD}	-500		500	V	CDM[4)]	P_4.1.10
ESD Susceptibility Pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750		750	V	CDM[4)]	P_4.1.11

1) Not subject to production test, specified by design.

2) Special care must be taken to control (e.g. by optical inspection) the proper handling of ST pin with an external resistor and not connecting directly to a higher voltage level, which allows an uncontrolled current flowing into the pin.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)

4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

Notes

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*
2. *Stresses above the ones listed her may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage	V_I	$V_Q + V_{dr}$	–	40	V	–	P_4.2.1
Output Voltage Range	V_Q	5	–	12	V	–	P_4.2.2
Current Sense Output Resistor	R_{CSO}	850	–	25.5 k	Ω	–	P_4.2.3
Current Sense Output Capacitor[1)]	C_{CSO}	1	–	4.7	µF	–	P_4.2.4
Junction Temperature	T_j	-40	–	150	°C	–	P_4.2.5
Output Capacitor Requirements[1)]	C_Q	1	–	–	µF	–[2)]	P_4.2.6
Output Capacitor Requirements[1)]	ESR_{CQ}	–	–	10	Ω	–[3)]	P_4.2.7

1) Not subject to production test, specified by design

2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

3) Relevant ESR value at f = 10 kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 3 Thermal Resistance [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Case...	R_{thJC}	–	8	–	K/W	measured to the exposed pad	P_4.3.1
Junction to Ambient	R_{thJA}	–	132	–	K/W	Footprint only[2)]	P_4.3.2
Junction to Ambient	R_{thJA}	–	59	–	K/W	300 mm² PCB heat sink area[2)]	P_4.3.3
Junction to Ambient	R_{thJA}	–	49	–	K/W	600 mm² PCB heat sink area[2)]	P_4.3.4
Junction to Ambient	R_{thJA}	–	42	–	K/W	2s2p PCB[3)]	P_4.3.5

1) Not subject to production test, specified by design

2) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 Voltage Regulator

5.1 Description Voltage Regulator

The output voltage V_Q is controlled by comparing the feedback voltage (V_{ADJ}) to an internal reference voltage and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor C_Q, the output capacitor ESR, the load current and the chip temperature. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the **Table 2 "Functional Range" on Page 7** have to be maintained. For stability details please refer to the typical performance graph "Output Capacitor Series Resistivity ESR_{CQ}" on **Page 11**. In addition the output capacitor may need to be sized larger to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general a buffered supply voltage is recommended for the device. For details see **Chapter 9.1**.

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events. The integrated safeguards consist of output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, an integrated safe operation monitor lowers the maximum output current input voltages above V_{BAT} = 22 V.

The thermal shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to a cycling behavior of the output voltage until the fault is removed. However, junction temperatures above 150 °C are outside the maximum ratings and therefore significantly reduce the IC lifetime.

The TLF4277-2 allows a negative supply voltage. However, several small currents are flowing into the IC increasing its junction temperature. This reverse current has to be considered for the thermal design, respecting that the thermal protection circuit is not operating during reverse polarity condition.

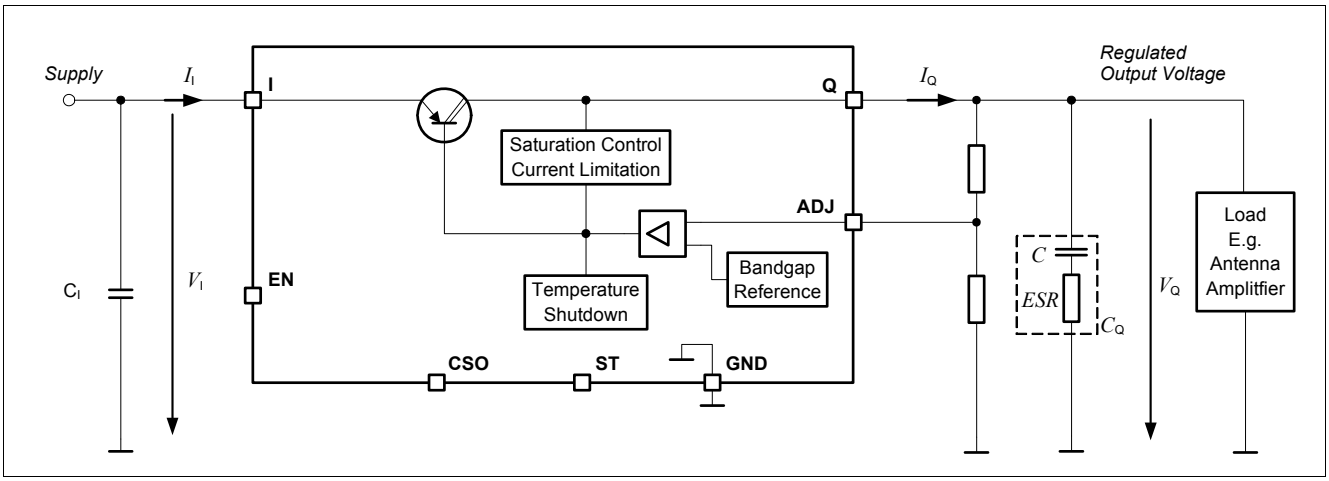


Figure 3 Block Diagram Voltage Regulator Circuit

5.2 Electrical Characteristics Voltage Regulator

Table 4 Electrical Characteristics: Voltage Regulator

V_{BAT} = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in Figure 9.1 “Application Diagram” on Page 20 (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Reference Voltage	$V_{REF,int}$	–	1.19	–	V	1)–	P_5.2.1
Output Voltage Tolerance 2)	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 300 mA; 9 V ≤ V_{BAT} ≤ 16 V 5 V ≤ V_Q ≤ 12 V with V_{BAT}> V_Q + 2V	P_5.2.2
Output Voltage Tolerance	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_{BAT} ≤ 16 V 5 V ≤ V_Q ≤ 12 V with V_{BAT} > V_Q + 1V	P_5.2.3
Output Voltage Tolerance	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 100 mA; 16 V ≤ V_{BAT} ≤ 32 V3) 5 V ≤ V_Q ≤ 12 V	P_5.2.4
Output Voltage Tolerance	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 10 mA; 32 V ≤ V_{BAT} ≤ 40 V3) 5 V ≤ V_Q ≤ 12 V	P_5.2.5
Load Regulation steady-state	$dV_{Q,load}$	- 30	- 5	–	mV	I_Q = 1 mA to 250 mA; V_{BAT} = 6 V; V_Q = 5 V	P_5.2.7
Line Regulation steady-state	$dV_{Q,line}$	–	5	20	mV	V_{BAT} = 6 V to 32 V; I_Q = 5 mA; V_Q = 5 V	P_5.2.8
Power Supply Ripple Rejection1)	$PSRR$	60	65	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; V_Q = 5 V; I_Q < 100 mA	P_5.2.9
Dropout Voltage V_{dr} = V_I - V_Q	V_{dr}	–	100	250	mV	I_Q = 100 mA4) VQ=5 V	P_5.2.10
Dropout Voltage V_{dr} = V_I - V_Q	V_{dr}	–	200	500	mV	I_Q = 200 mA4) VQ=5 V	P_5.2.11
Output Current Limitation	$I_{Q,max}$	301	–	700	mA	0 V ≤ V_Q ≤ 0.95 * $V_{Q,nom}$	P_5.2.13
Reverse Current	I_Q	-2	-1	–	mA	V_{BAT} =0 V; V_Q = 5 V	P_5.2.14
Reverse Current at Negative Input Voltage	I_{BAT}	-10	-6	–	mA	V_{BAT} = -16 V; V_Q = 0 V	P_5.2.15
Overtemperature Shutdown Threshold	$T_{j,sd}$	151	–	200	°C	T_j increasing1)	P_5.2.16
Overtemperature Shutdown Threshold Hysteresis	$T_{j,hy}$	–	15	–	K	T_j decreasing1)	P_5.2.17

1) Parameter not subject to production test; specified by design.

2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.

3) See typical performance graph for details.

4) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

5.3 Application Information for setting the variable output voltage

The output voltage of the TLF4277-2 can be adjusted between 5 V and 12 V by an external output voltage devider, closing the control loop to the voltage adjust pin ADJ.

The voltage at pin ADJ is compared to the internal reference of typical 1.19 V in an error amplifier. It controls the output voltage.

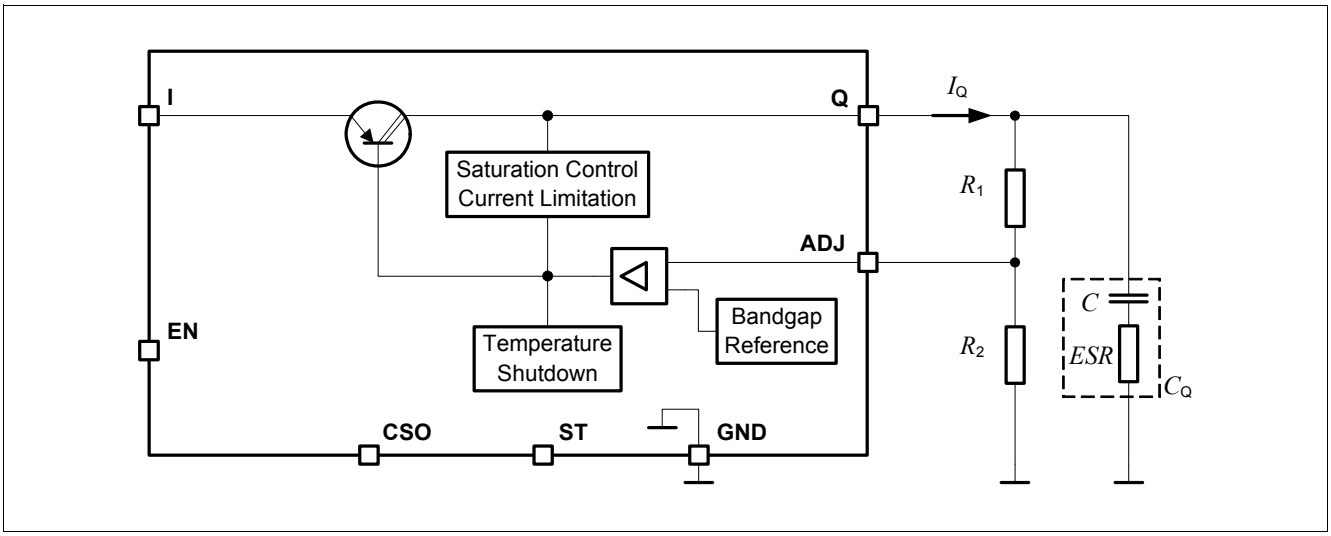


Figure 4 Application Detail External Components at Output for Variable Voltage Regulator

The output voltage is calculated according to **Equation (1)**:

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (1)$$

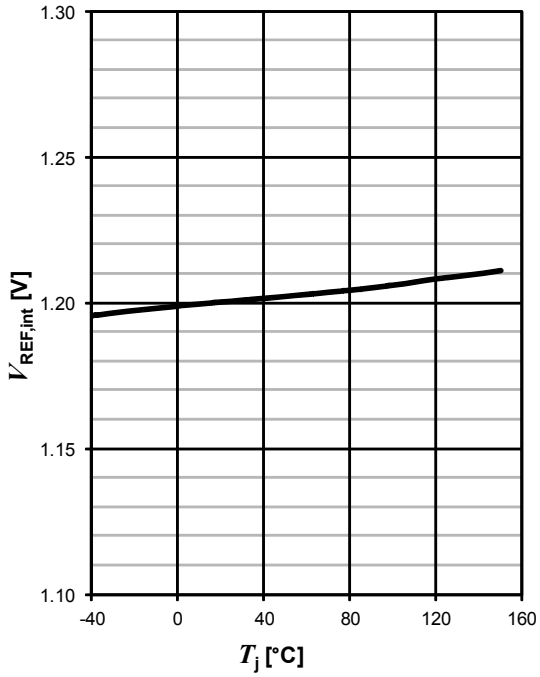
$V_{REF,int}$ is typically 1.19 V.

To avoid errors caused by leakage current I_{ADJ}, we recommend to choose the resistor value for R_2 < 27 kΩ.

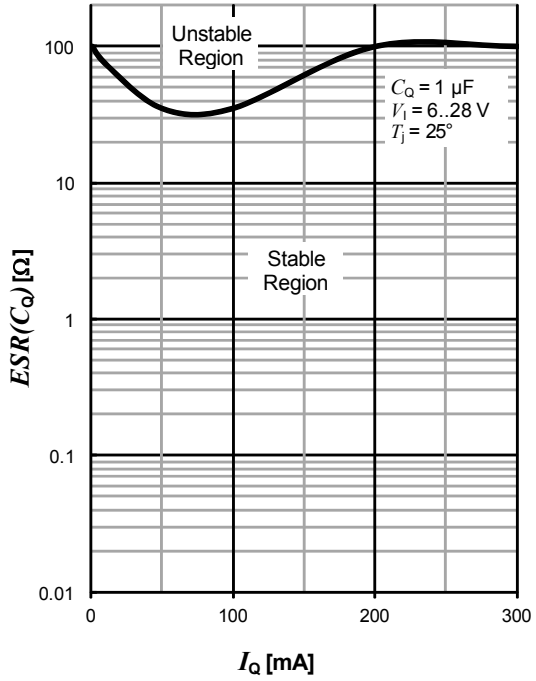
The accuracy of the resistors for the external voltage divider can lead to a higher tolerance of the output voltage. To achieve a reasonable accuracy resistors with a tolerance of 1% or lower are recommended for the feedback divider.

5.4 Typical Performance Characteristics Voltage Regulator

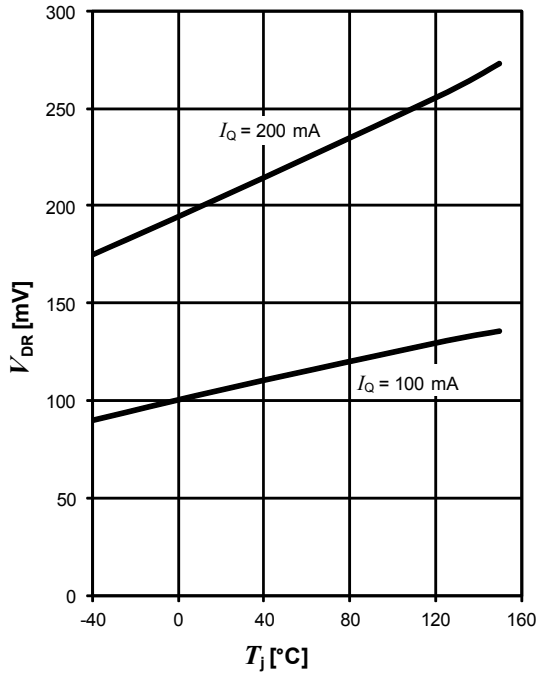
Reference Voltage $V_{REF,int}$ vs. Junction Temperature T_j



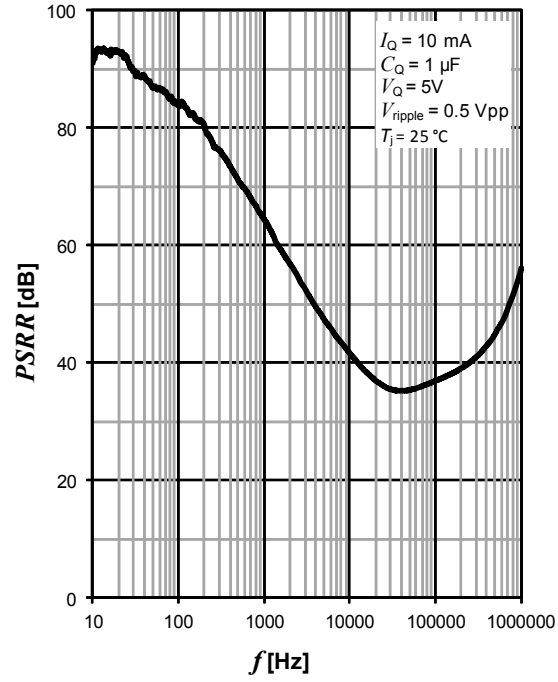
Output Capacitor Series Resistivity ESR_{CQ} vs. Output Current I_Q



Dropout Voltage V_{dr} vs. Junction Temperature T_j



Power Supply Ripple Rejection $PSRR$



6 Current Consumption

6.1 Electrical Characteristics Current Consumption

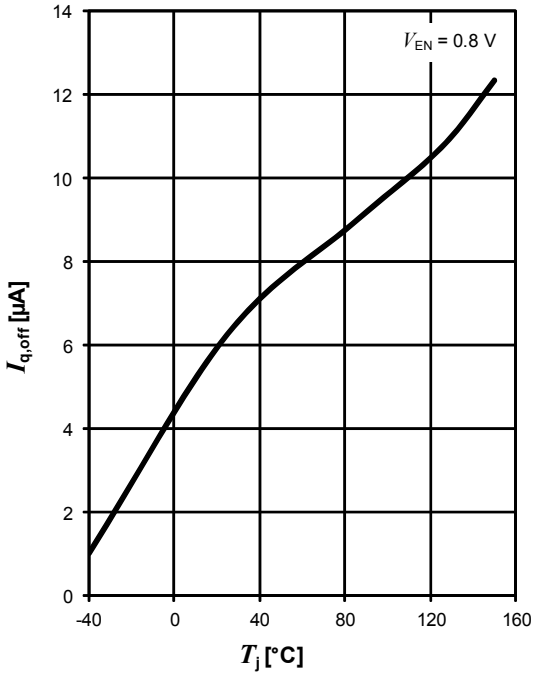
Table 5 Electrical Characteristics: Current Consumption

V_{BAT} = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground; direction of currents as shown in **Figure 9.1 "Application Diagram" on Page 20** (unless otherwise specified)

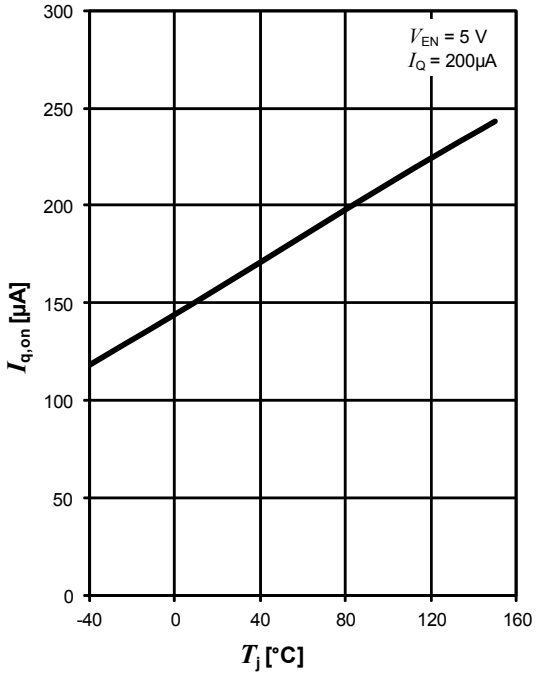
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption	$I_{q,on}$	–	150	200	µA	I_Q ≤ 200 µA ; T_j ≤ 25 °C; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.1
Current Consumption	$I_{q,on}$	–	–	250	µA	I_Q ≤ 200 µA; T_j ≤ 85 °C; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.2
Current Consumption	$I_{q,on}$	–	1.2	2.6	mA	I_Q = 50 mA; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.3
Current Consumption	$I_{q,on}$	–	5.5	11	mA	I_Q = 200 mA; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.4
Current Consumption	$I_{q,off}$	–	–	3	µA	T_j ≤ 25 °C; V_{EN} = 0 V $I_q = I_I - I_Q$	P_6.1.5
Current Consumption	$I_{q,off}$	–	–	5	µA	T_j ≤ 85 °C; V_{EN} = 0 V $I_q = I_I - I_Q$	P_6.1.6
Current Consumption	$I_{q,off}$	–	–	15	µA	T_j ≤ 85 °C; V_{EN} = 0.8 V $I_q = I_I - I_Q$	P_6.1.7

6.2 Typical Performance Graphs Current Consumption

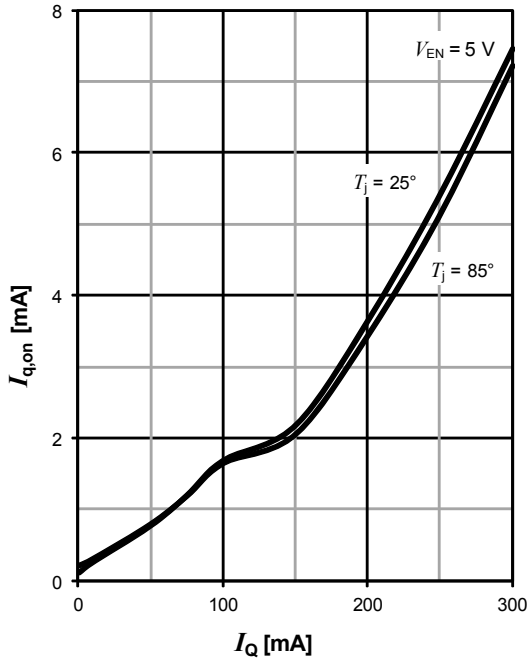
Current Consumption $I_{q,off}$ vs. Junction Temperature T_j



Current Consumption $I_{q,on}$ vs. Junction Temperature T_j



Current Consumption $I_{q,on}$ vs. Output Current I_Q



7 Current and Protection Monitor Functions

7.1 Functional Description Current and Protection Monitors

The TLF4277-2 provides a set of advanced monitor functionality. The current flowing out of the power stage can be monitored at the CSO output. In addition the current limitation can be adjusted via external resistor. Events of the implemented protection functions are reported through dedicated voltage levels at the CSO output. This information can be processed by an external µC for system analysis and failure identification. The monitored events are over-current, overvoltage, and temperature shutdown. In addition all three fault conditions are routed also to the digital output pin ST.

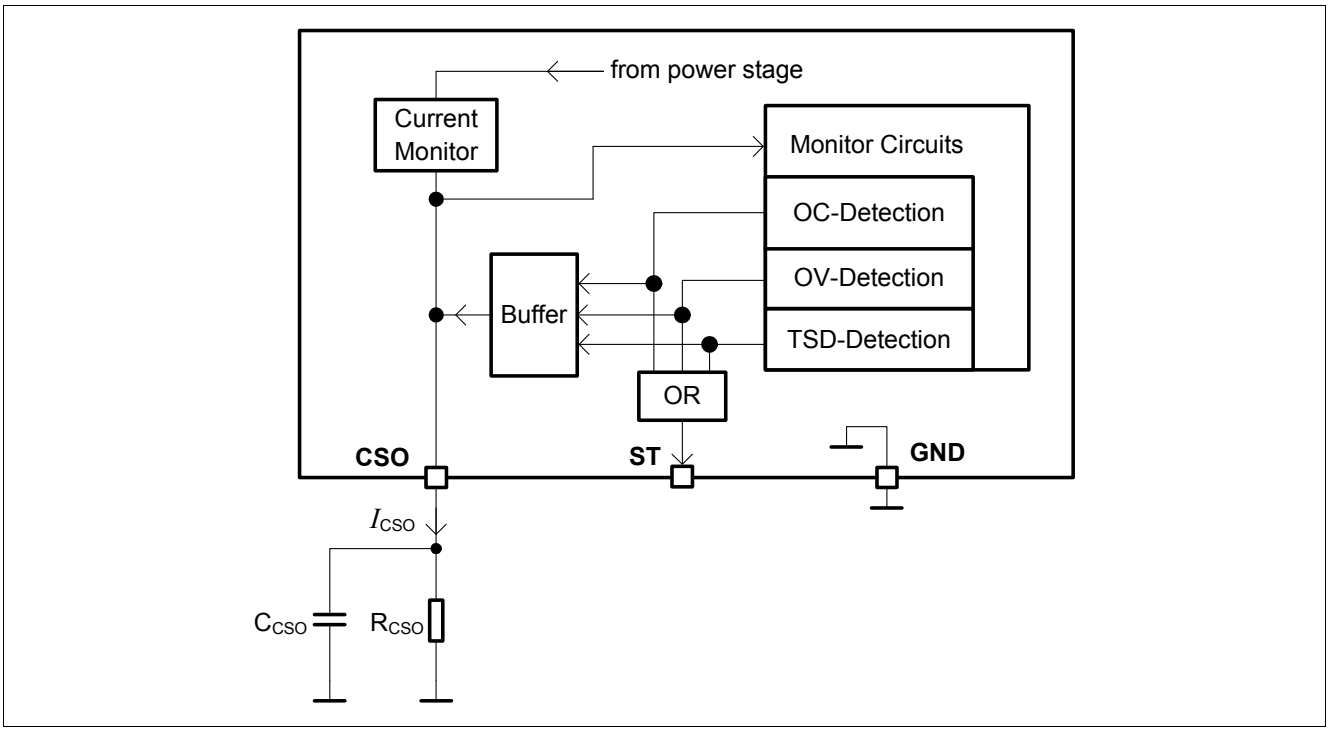


Figure 5 Block diagram current and protection monitor

To reduce possible effects from the supply voltage V_{BAT} additional filtering of the supply voltage is recommended. A 100 nF capacitor should be placed as close a possible to the IC terminal, which is connected to V_{BAT}.

Figure 6 shows the output level at the CSO pin versus the operation or fault condition. The graph is valid for the following set up of external components:

C_{CSO} = 2.2 µF

R_{CSO} = 1.5 kΩ

Note: In case of high input voltage (V_I > 20 V), high junction temperature (T_j > 151°C) and CSO pin is directly connected to GND without resistor, the return to normal operation from the "thermal shutdown mode" can't be ensured.

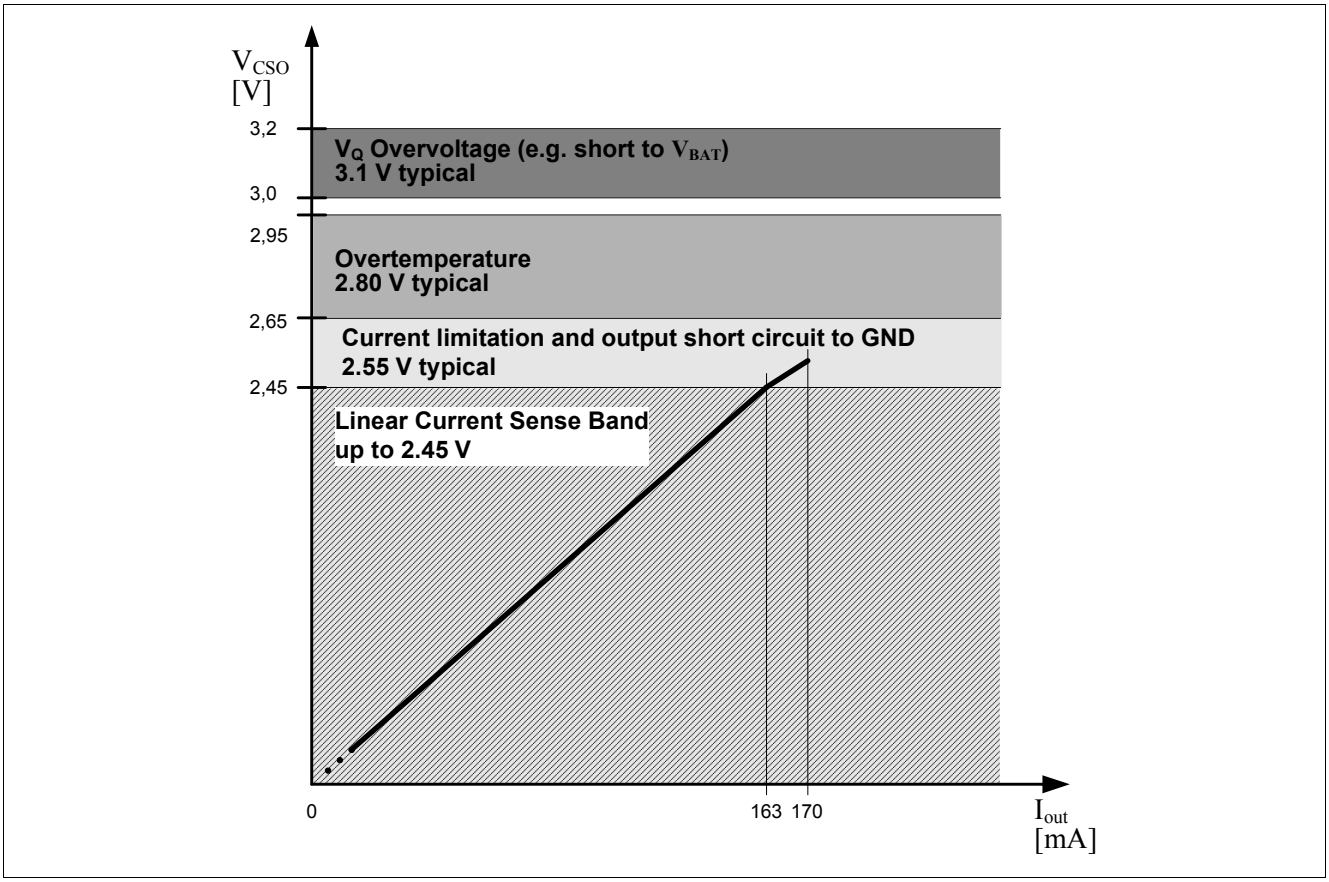


Figure 6 Output levels and functionality of the CSO output

Note: The graph is just an example and only valid for an certain configuration of the external components.

7.1.1 Linear Current Monitor

Inside the linear current monitor area the current driven out of the CSO pin is direct proportional to the output current (IQ).

The level of the current I_{CSO} can be calculated according to **Equation (2)**:

(2)

$$I_{CSO} = \frac{I_Q}{F_{IQ/ICSO}}$$

7.1.2 Adjustable Output Current Limitation

The TLF4277-2 has an adjustable current limitation for the current flowing out of the power stage. If the level of the output current exceeds the defined current limit threshold (IQ,lim), the output current of the TLF4277-2 will be limited.

Setting of the adjustable current limitation: (3)

$$I_{Q,lim} = \frac{2.55V \times F_{IQ/ICSO}}{R_{CSO}}$$

A voltage level as defined in **"CSO Voltage Level" on Page 17** will be applied at the CSO pin. In addition the ST pin will be set low.

*Note: During power up of the device, the regulator works in output current limitation. Regardless if the output current is limited by the protection function according to **"Output Current Limitation" on Page 9**, or by the adjustable output current limitation according to **"Adjustable Current Limit" on Page 17**. If an adjustable current limit is set, the status output pin ST is set to low as long as the adjustable current limitation is active during power up sequence.*

Example: To achieve a current limitation of e.g. 170mA the following configuration can be used:

$$I_{Q,lim} = \frac{2.55V \times 100}{1.5k\Omega} = 170mA$$

$F_{IQ/ICSO}$ = 100

R_{CSO} = 1.5 kΩ

7.1.3 Overvoltage Detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277-2 has an overvoltage detection implemented. An overvoltage will be detected, if the voltage level at the ADJ pin is 20% higher than the internal reference voltage $V_{REF,int}$ defined in **"Reference Voltage" on Page 9**.

In case of overvoltage the CSO pin will set to a voltage level as defined in **"CSO Voltage Level" on Page 17**. In addition the ST pin will be set low.

7.1.4 Thermal Shutdown Detection

If the junction temperature will exceed the limits defined in the **"Overtemperature Shutdown Threshold" on Page 9** the TLF4277-2 will disable the output voltage. In this case a voltage level as defined in **"CSO Voltage Level" on Page 17** will be applied at the CSO pin. In addition the ST pin will be set low.

7.1.5 Status Output Signal

The status condition pin ST is an open collector output. An external pull-up resistor has to be applied for functionality and to limit the current into the pin (e.g. connect via a resistor to "Q"). Connecting the ST pin directly to a supply voltage may damage the device.

Is one or more of the monitored protection functions (over-current, overvoltage and temperature shutdown) activated, the digital Status Output pin ST is set to "low".

Table 6 Electrical Characteristics: Current Monitor Function

V_{BAT} = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in Figure 9.1 “Application Diagram” on Page 20 (unless otherwise specified)

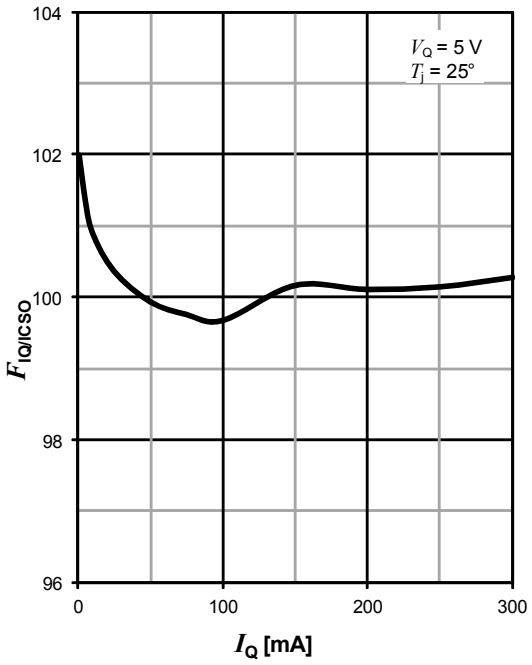
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Linear Current Monitor							
Current Monitor Factor Factor = I_Q /I_{CSO} (I_Q = 10 mA - 150 mA)	$F_{IQ/ICSO}$	95	100	105	–	T_j = -40° to 125°C V_{IN}= 9 V to 16 V V_Q = 5 V to 12 V V_{IN} > V_Q + 2.0 V[1)]	P_7.1.1
Current Monitor Factor Factor = I_Q /I_{CSO}	$F_{IQ/ICSO}$	90	100	110	–	1 mA ≤ I_Q ≤ 300 mA V_Q = 5 V	P_7.1.5
CSO current at no load condition	$I_{CSO,off}$	–	–	550	nA	no load connected at Q R_2 = 27 kΩ V_Q = 5 V	P_7.1.6
Adjustable Current Limitation							
Adjustable Current Limit Range	$I_{Q,lim}$	10	-	300	mA	850 Ω < R_{CSO} < 25.5 kΩ V_Q < 0,95 * $V_{Q,nom}$[1)]	P_7.1.7
Adjustable Current Limit Tolerance	$I_{Q,lim}$	-10	–	10	%	10 mA ≤ $I_{Q,lim}$ ≤ 300 mA T_j = -40° to 125°C 0.95*$V_{Q,nom}$ > V_Q > 3.0 V	P_7.1.8
Adjustable Current Limit Tolerance	$I_{Q,lim}$	-10	–	25	%	10 mA ≤ $I_{Q,lim}$ ≤ 300 mA T_j = -40° to 125°C 0.95*$V_{Q,nom}$ > V_Q > 0 V	P_7.1.15
CSO Voltage Level Current limitation	V_{CSO,cur_lim}	2.45	2.55	2.65	V	V_Q < 0,95 * $V_{Q,nom}$[1)]	P_7.1.9
Output Level Overvoltage Detected							
CSO Voltage Level Overvoltage detected	$V_{CSO,OV}$	3.0	3.1	3.2	V	V_{ADJ} > 1.2 * $V_{REF,nom}$[1)]	P_7.1.10
Output Level Overtemperature Detected							
CSO Voltage Level Overtemperature Detected [2)]	$V_{CSO,TSD}$	2.65	2.8	2.95	V	151 °C < T_j < 180 °C	P_7.1.12
Status Output Signal							
Status Output Digital Signal Low Voltage	$V_{ST,low}$	–	0.2	0.4	V	I_{ST} ≤ 1.8 mA	P_7.1.13
Status Output Digital Signal Sink current	I_{ST}	–	–	1.8	mA	–	P_7.1.14

1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation

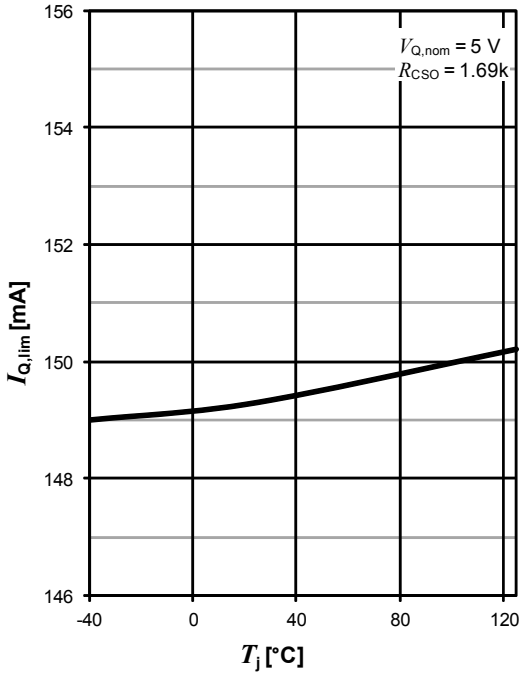
2) Specified by design; not subject to production test

7.1.6 Typical Performance Graphs Current Monitor

Current Monitor Factor $F_{IQ/ICSO}$ vs. Output Current I_Q



External Current Limitation $I_{Q,lim}$ vs. Junction Temperatur T_j



8 Enable Function

8.1 Description Enable Function

The TLF4277-2 can be turned on or turned off via the EN Input. With voltage levels higher than $V_{EN,high}$ applied to the EN Input the device will be completely turned on. A voltage level lower than $V_{EN,low}$ sets the device to low quiescent current mode. In this condition the device is turned off and is not functional. The Enable Input has a build in hysteresis to avoid toggling between ON/OFF state, if signals with slow slope are applied to the input. Enable input pin has an internal pull down resistor.

8.2 Electrical Characteristics Enable Function

Table 7 Electrical Characteristics: Enable Function

V_{BAT} = 13.5 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, direction of currents as shown in Figure 9.1 “Application Diagram” on Page 20 (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Enable Low Signal Valid	$V_{EN,low}$	–	–	0.8	V	–	P_8.2.1
Enable High Signal Valid	$V_{EN,high}$	2	–	–	V	see also startup time P_8.2.7	P_8.2.2
Enable Threshold Hysteresis	$V_{EN,hyst}$	50	–	–	mV	–	P_8.2.3
Enable Input current	$I_{EN,high}$	–	–	5	µA	V_{EN} = 5 V	P_8.2.4
Enable Input current	$I_{EN,high}$	–	–	20	µA	V_{EN} < 18 V	P_8.2.5
Enable internal pull-down resistor	R_{EN}	0.94	1.5	2.5	MΩ	V_{EN} < 5 V	P_8.2.6
Startup time	t_{EN}	–	180	–	µs	C_Q = 1 µF; $V_{Q,nom}$ = 5 V; $I_{Q,load}$ = 150 mA; time from V_{EN} > 2 V (0 V to 5 V transition) till V_Q = 90 % of $V_{Q,nom}$	P_8.2.7

9 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

9.1 Application Diagram

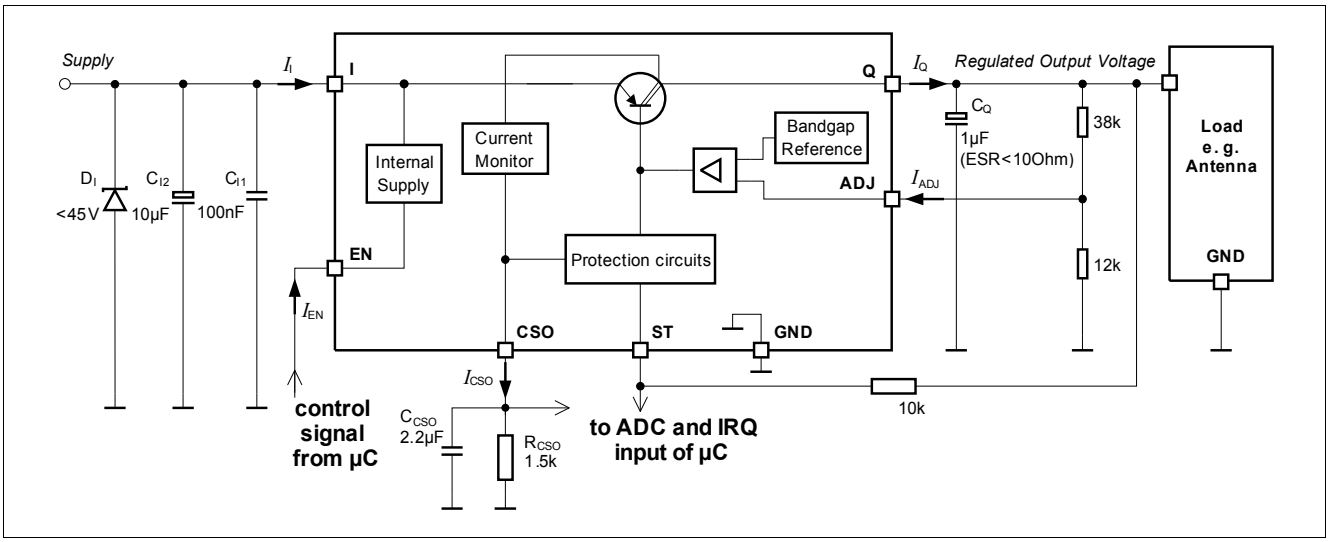


Figure 7 Application Diagram

9.2 Selection of External Components

9.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

9.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **"Functional Range" on Page 7**. The graph **"Output Capacitor Series Resistivity ESR_{CQ} vs. Output Current I_Q" on Page 11** shows the stable operation range of the device.

TLF4277-2 is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

9.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (4)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (5)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal Resistance" on Page 7**.

Example

Application conditions:

V_I = 13.5V

V_Q = 5V

I_Q = 100mA

T_a = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I – V_Q) \times I_Q + V_I \times I_q$

= (13.5V – 5V) × 100mA + 13.5V × 5.0mA

= 0.850W + 0.068W

= 0.918W

$R_{thJA,max} = (T_{j,max} – T_a) / P_D$

= (150°C – 85°C) / 0.918W = 70.8K/W

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 70.8 K/W. According to **"Thermal Resistance" on Page 7**, at least 300 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

9.4 Reverse Polarity Protection

TLF4277-2 is self protected against reverse polarity faults and allows negative supply voltage. External reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **"Absolute Maximum Ratings" on Page 6** must be kept.

The reverse voltage causes several small currents to flow into the IC hence increasing its junction temperature. As the thermal shut down circuitry does not work in the reverse polarity condition, designers have to consider this in their thermal design.

9.5 Further Application Information

- For further information you may contact **http://www.infineon.com/**

10 Package Outlines

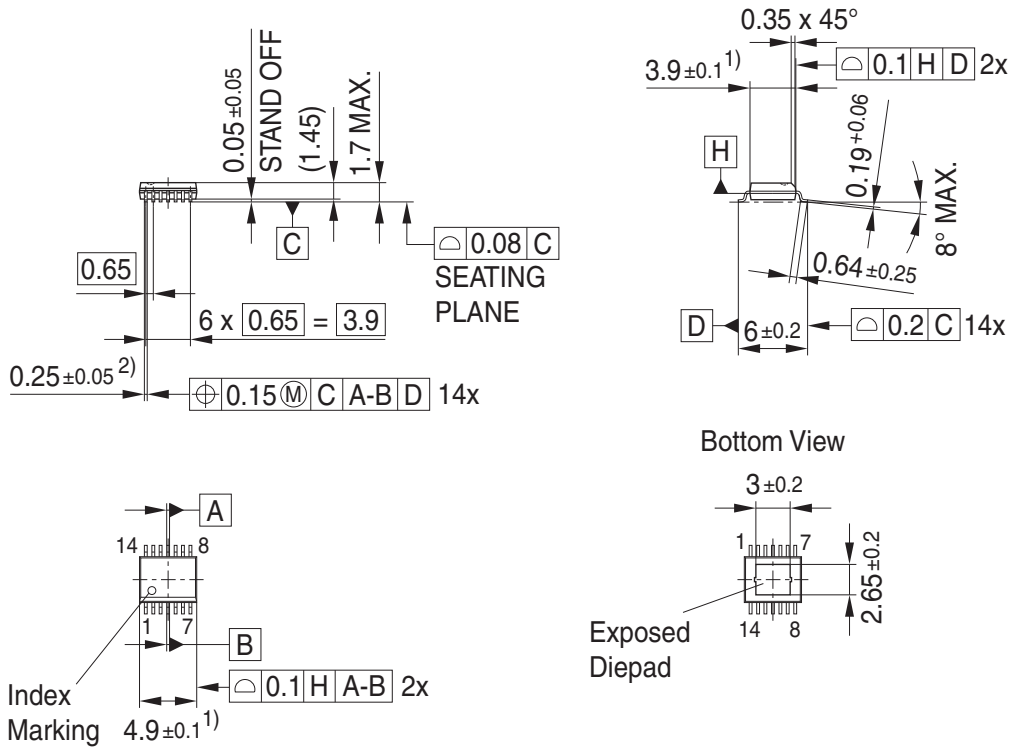


Figure 8 PG-SSOP14 EP

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

11 Revision History

Revision	Date	Changes
1.0	2014-03-13	Initial version

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