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## P-Channel PowerTrench<sup>®</sup> MOSFET

## -30 V, -122 A, 3.2 mΩ

## Features

- Max  $r_{DS(on)}$  = 3.2 m $\Omega$  at  $V_{GS}$  = -10 V,  $I_D$  = -21.1 A
- Max  $r_{DS(on)}$  = 5.0 m $\Omega$  at V<sub>GS</sub> = -4.5 V, I<sub>D</sub> = -15.7 A
- Advanced Package and Silicon combination for low r<sub>DS(on)</sub>
- HBM ESD Protection Level of 8kV Typical(Note 3)
- MSL1 Robust Package Design
- RoHS Compliant

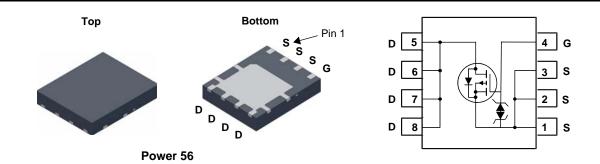


## **General Description**

The FDMS6681Z has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  and ESD protection.

## Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



## MOSFET Maximum Ratings T<sub>A</sub> = 25 °C unless otherwise noted.

Symbol	Parar	neter		Ratings	Units
V <sub>DS</sub>	Drain to Source Voltage			-30	V
V <sub>GS</sub>	Gate to Source Voltage			±25	V
I <sub>D</sub>	Drain Current -Continuous	T <sub>C</sub> = 25 °C	(Note5)	-122	
	-Continuous	T <sub>C</sub> = 100 °C	(Note5)	-77	А
	-Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	-21.1	A
	-Pulsed		(Note4)	-600	
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> = 25 °C		73	w
	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.5	vv
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Tempe	rature Range		-55 to +150	°C

## **Thermal Characteristics**

$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case	1.7	°C/W
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient (Note 1	a) 50	C/VV

## Package Marking and Ordering Information

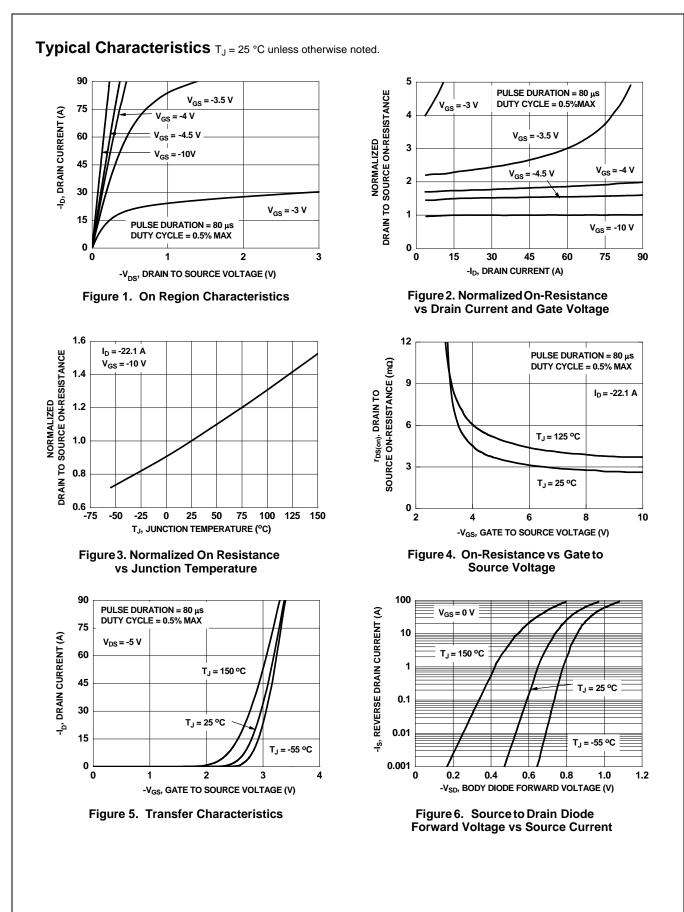
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS6681Z	FDMS6681Z	Power 56	13 "	12 mm	3000 units

June 2015

	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	octeristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = -250 μA, V <sub>GS</sub> = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250 \ \mu$ A, referenced to 25 °C		20		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 25 \text{ V}, V_{DS} = 0 \text{ V}$			±10	μA
On Chara	cteristics					
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = -250 \ \mu A$	-1	-1.7	-3	V
$\frac{\Delta V_{\text{GS(th)}}}{\Delta T_{\text{J}}}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu A,$ referenced to 25 °C		-7		mV/°C
	· · ·	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -22.1 A		2.7	3.2	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -15.7 A		4.0	5.0	mΩ
		$V_{GS}$ = -10 V, I <sub>D</sub> = -22.1 A, T <sub>J</sub> = 125 °C		3.9	5.0	
9 <sub>FS</sub>	Forward Transconductance	V <sub>DD</sub> = -10 V, I <sub>D</sub> = -22.1 A		143		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance			7803	10380	pF
C <sub>oss</sub>	Output Capacitance	<sup>ー</sup> V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, – f = 1 MHz		1540	2050	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			1345	2020	pF
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub>	Turn-On Delay Time Rise Time Turn-Off Delay Time	$V_{DD}$ = -15 V, I <sub>D</sub> = -22.1 A, V <sub>GS</sub> = -10 V, R <sub>GEN</sub> = 6 Ω		15 38 260	24 61 416	ns ns ns
t <sub>f</sub>	Fall Time			197	316	ns
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> = 0 V to -10 V		172	241	nC
Q <sub>g</sub>	Total Gate Charge	$V_{GS} = 0 V \text{ to } -5 V$ $V_{DD} = -15 V,$		97	136	nC
Q <sub>gs</sub>	Gate to Source Charge	$I_{\rm D} = -22.1  {\rm A}$		22		nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge			46		nC
•	urce Diode Characteristics		1	1	4	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = -2.1 A$ (Note 2)		0.68	1.2	V
50		$V_{GS} = 0 V, I_S = -22.1 A$ (Note 2)		0.79	1.25	V
t <sub>rr</sub>	Reverse Recovery Time	- I <sub>F</sub> = -22.1 A, di/dt = 100 A/μs		44	71	ns
Q <sub>rr</sub>	Reverse Recovery Charge			39	63	nC

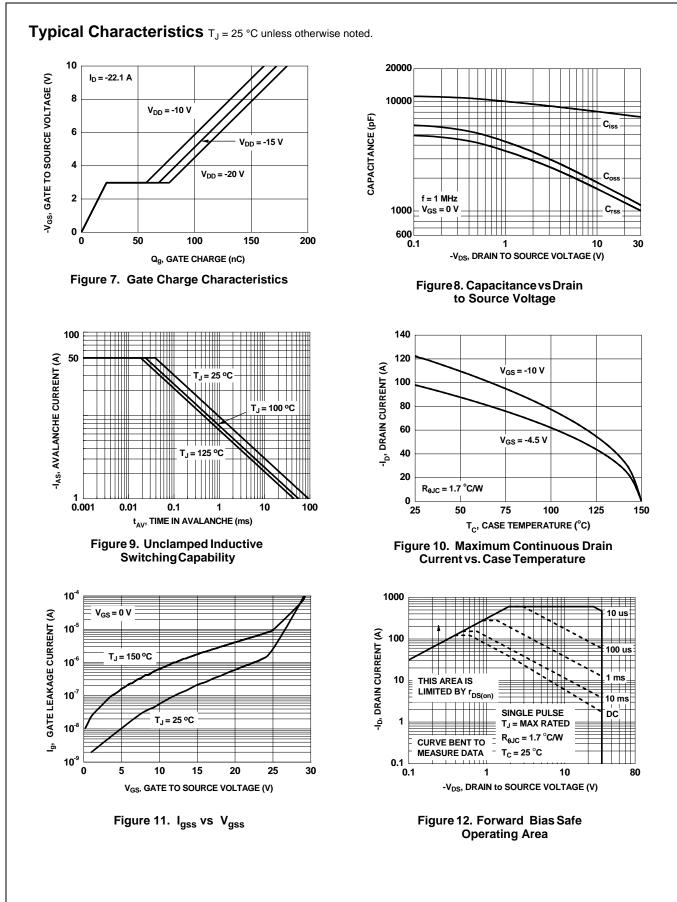
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Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.</li>
The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
Pulsed Id please refer to Fig 12 SOA graph for more details.
Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal electro-mechanical application board design.

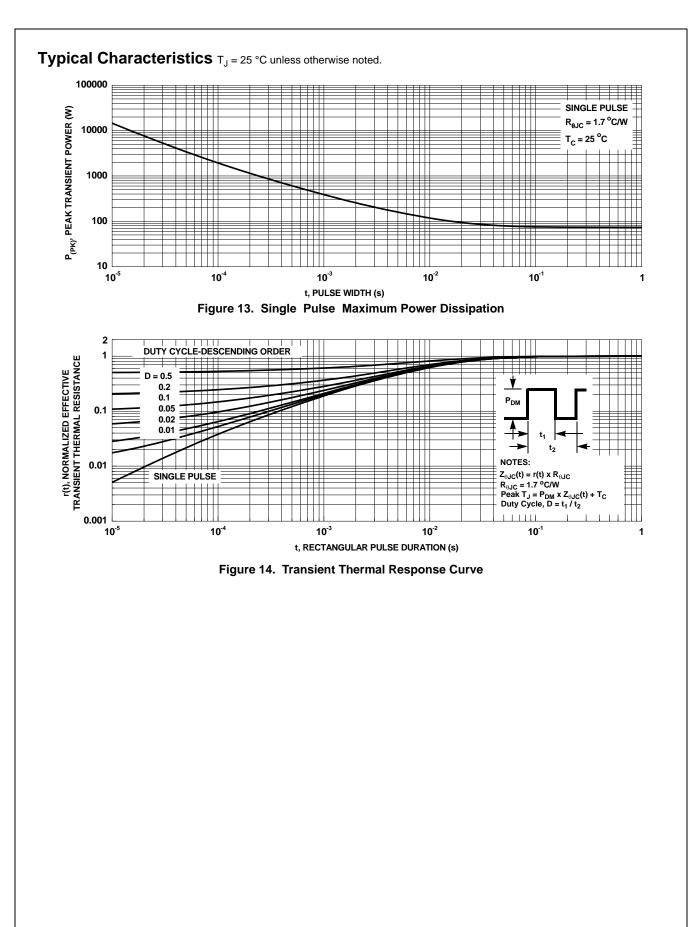


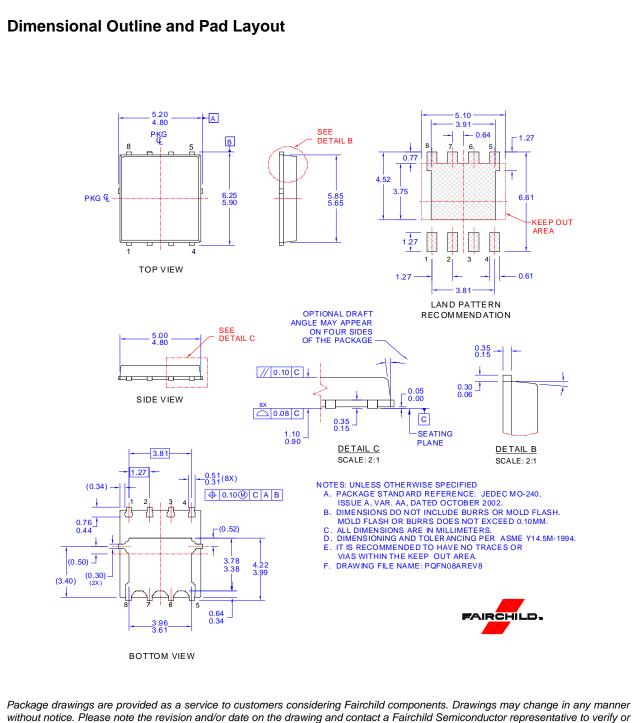
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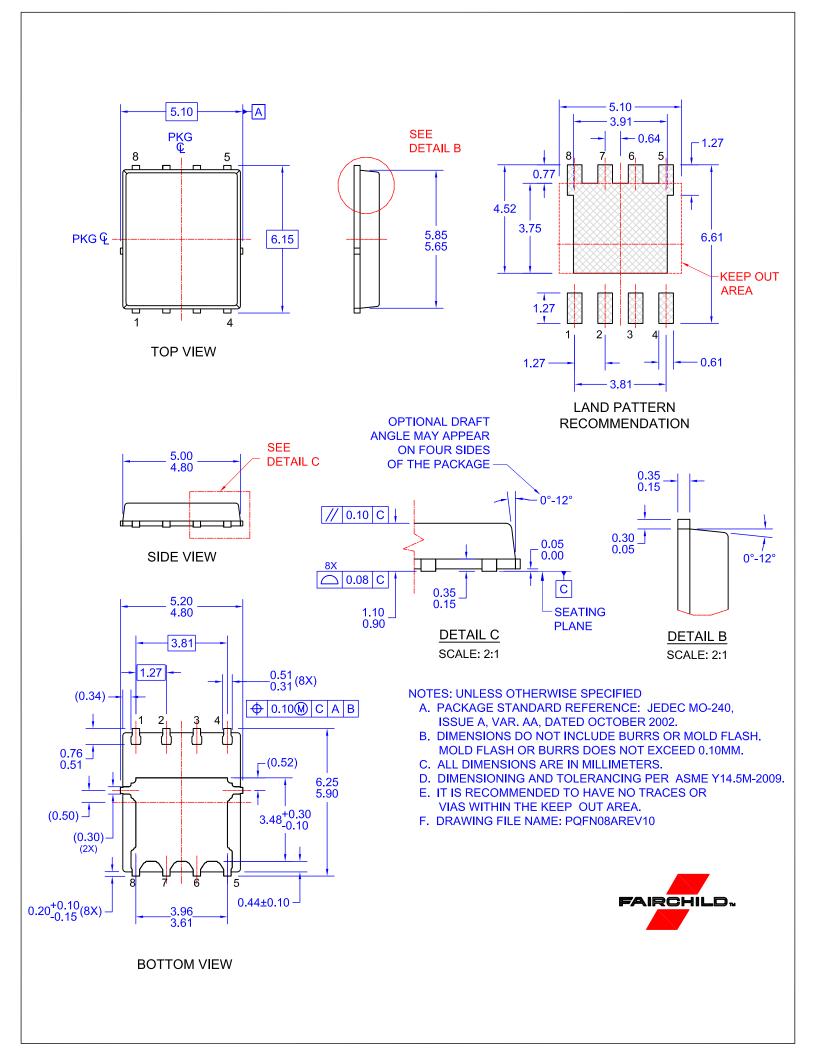
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